Electronic Version
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Claims

[c1] 1. A method for fabricating a non-volatile memory, comprising:
forming a linear conductor on a substrate, interposed by a gate dielectric layer;
forming a trapping layer on the substrate and two sidewalls of the linear conductor;
forming two conductive spacers on the two sidewalls of the linear conductor, interposed by the trapping layer;
forming a buried drain in the substrate outside each conductive spacer;
forming a buried drain insulator on the buried drain;
forming a conductive layer over the substrate; and
patterning the conducive layer, the linear conductor and the conductive spacers to form a word line and a gate electrically connected with the word line.

[c2] 2. The method of claim 1, wherein the steps of forming the buried drain insulator and forming the conductive layer comprise:
forming an insulating layer on the linear conductor and the buried drain;
forming a protective layer on the insulating layer on the

buried drain;
removing the insulating layer on the linear conductor using the protective layer as a mask, while the remaining insulating layer is the buried drain insulator;
removing the protective layer; and
forming the conductive layer over the substrate contacting with the linear conductor and the conductive spacers.

[c3] 3. The method of claim 2, wherein the protective layer comprises a bottom anti-reflection coating (BARC).

[c4] 4. The method of claim 2, wherein the insulating layer comprises a thermal oxide layer.

[c5] 5. The method of claim 4, wherein the thermal oxide is formed with a thermal oxidation process that also produces a gate oxide layer in a peripheral area of the non-volatile memory.

[c6] 6. The method of claim 5, wherein the conductive layer is also formed on the peripheral area, and is defined to form the word line and simultaneously a gate electrode in the peripheral area.

[c7] 7. The method of claim 1, wherein the trapping layer comprises an ONO composite layer.

[c8] 8. The method of claim 1, wherein the gate dielectric

layer is an oxide layer extending beyond the linear conductor before the trapping layer is formed, and the trapping layer is an NO composite layer.

[c9] 9. The method of claim 1, wherein the conducive layer, the linear conductor and the conductive spacers comprise doped polysilicon.

[c10] 10. The method of claim 1, wherein the gate dielectric layer comprises SiO_2.

[c11] 11. A method for fabricating a non-volatile memory, comprising:
forming a plurality of parallel linear conductors on a substrate, each of which being separated from the substrate by a gate dielectric layer;
forming two L-shaped trapping layers along sidewalls of each linear conductor;
forming a buried drain in the substrate between each two linear conductors;
forming a buried drain insulator on each buried drain;
forming a conductive layer over the substrate; and
patterning the conducive layer and the linear conductors to form a plurality of word lines and a plurality of gates electrically connected with the word lines.

[c12] 12. The method of claim 11, wherein the step of forming

two L-shaped trapping layers along the sidewalls of each linear conductor comprises:

forming a substantially conformal trapping layer over the substrate;

forming two conductive spacers on the sidewalls of each linear conductor, interposed by the trapping layer; and

removing portions of the substantially conformal trapping layer exposed by the conductive spacers.

[c13] 13. The method of claim 11, wherein the steps of forming the buried drain insulator and forming the conductive layer comprise:

forming an insulating layer on the linear conductors and the buried drains;

forming a protective layer on the insulating layer on the buried drains;

removing the insulating layer on the linear conductors using the protective layer as a mask, while the remaining insulating layer is the buried drain insulator;

removing the protective layer; and

forming the conductive layer over the substrate contacting with the linear conductors.

[c14] 14. The method of claim 13, wherein the protective layer comprises a bottom anti-reflection coating (BARC).

[c15] 15. The method of claim 13, wherein the insulating layer

comprises a thermal oxide layer.

[c16] 16. The method of claim 15, wherein the thermal oxide is formed with a thermal oxidation process that also produces a gate oxide layer in a peripheral area of the non-volatile memory.

[c17] 17. The method of claim 16, wherein the conductive layer is also formed on the peripheral area, and is defined to form the word lines and simultaneously a gate electrode in the peripheral area.

[c18] 18. The method of claim 11, wherein each L-shaped trapping layer comprises an ONO composite layer.

[c19] 19. The method of claim 11, wherein the gate dielectric layer is an oxide layer extending beyond the linear conductors before the L-shaped trapping layers are formed, and each L-shaped trapping layer is an NO composite layer.

[c20] 20. The method of claim 11, wherein the conducive layer and the linear conductors comprise doped polysilicon.

[c21] 21. A non-volatile memory device, comprising:
a substrate;
a gate dielectric layer on the substrate;
a gate on the gate dielectric layer;

two L-shaped trapping layers on sidewalls of the gate and on the substrate;
two conductive spacers on the sidewalls of the gate, separated from the gate and the substrate by the L-shaped trapping layers;
two doped regions in the substrate beside the conductive spacers; and
a word line over the substrate, contacting with the conductive spacers and top of the gate.

[c22] 22. The non-volatile memory device of claim 21, wherein each L-shaped trapping layer comprises an ONO composite layer.

[c23] 23. The non-volatile memory device of claim 21, wherein the gate dielectric layer comprises an oxide layer.

[c24] 24. The non-volatile memory device of claim 21, wherein the word line, the gate and the conductive spacers comprise doped polysilicon.

[c25] 25. A non-volatile memory array, comprising:
a substrate;
a plurality of gate structures arranged in rows and columns, each comprising
a gate dielectric layer on the substrate;
a gate on the gate dielectric layer;

two L-shaped trapping layers on sidewalls of the gate and the substrate; and

two conductive spacers on the sidewalls of the gate, separated from the gate and the substrate by the two L-shaped trapping layers;

a plurality of buried drains, each between two columns of gate structures; and

a plurality of word lines over the substrate, each contacting with the two conductive spacers and top of the gate of each of the gate structures in one row.

[c26] 26. The non-volatile memory array of claim 25, wherein each L-shaped trapping layer comprises an ONO composite layer.

[c27] 27. The non-volatile memory array of claim 25, wherein the gate dielectric layer comprises an oxide layer.

[c28] 28. The non-volatile memory array of claim 25, wherein the word lines, the gates and the conductive spacers comprise doped polysilicon.